

Time: 3Hours

- N.B: (1) Question No.1 is compulsory.
(2) Solve any three questions from the remaining five.
(3) Figures to the right indicate full marks
(4) Assume suitable data if required and mention the same in the answer sheet.

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1 Solve any four

- (a) Draw basic current mirror and derive expression for output current I_o in terms of reference current I_{REF} .
- (b) For the single stage resistive load CS amplifier as shown in Fig. 1b. $V_{DD}=5V$, $V_{TN}=0.5V$, $\mu_n C_{ox}=100\mu A/(V^2)$, $(W/L)=70$ and $R_D=1K$. Find input voltage swing and corresponding output voltage swing.

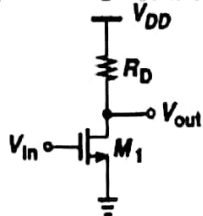


Fig. 1b

- (c) For NMOS device with $W=100\mu m$, $L=0.5\mu m$, $g_m=10mS$, the $1/f$ noise corner frequency is measured to be $500kHz$. If $\tau_{ox}=90A^0$, what is flicker noise coefficient 'K' in this technology.
- (d) What is thermal noise? How to model the same in MOSFET
- (e) Discuss various performance parameters of Comparator.

2 (a) Explain design procedure to design 2 stage Operational trans conductance amplifier (OTA) using appropriate equations to meet the specifications like Voltage gain (A_v), Gain Bandwidth (GB), Slew Rate (SR), Power Dissipation (P_{diss}), Input Common Mode Range (ICMR), Output Voltage Range. 15

(b) Why frequency compensation is necessary for operational amplifier. Explain Miller's compensation technique with respect to two stage OTA. 5

3 (a) Explain in detail working of switched capacitor Amplifier with neat circuit diagram and appropriate waveforms. 10

(b) Design current mirror load differential amplifier to meet the following specifications 10
small-signal differential voltage gain $A_v > 100V/V$, higher cut-off frequency $f_{3db} \geq 150kHz$, Slew Rate $SR \geq 10V/\mu s$, $C_L = 5pF$, Input common Mode Range (ICMR) = -1.0V to 2.5V, Power Dissipation $P_{diss} \leq 2mW$, $V_{DD} = 3.5V$, $V_{SS} = -3.5V$. Use transistors with $V_{TN} = 0.7V$, $\mu_n C_{ox} = 120\mu A/V^2$, $\lambda_n = 0.04V^{-1}$, $V_{TP} = -0.7V$, $\mu_p C_{ox} = 60\mu A/V^2$, $\lambda_p = 0.05V^{-1}$

Turn Over

- 4 (a) Explain with the help of suitable example why input referred noise modeled by single voltage source in series with input is incomplete representation of noise at the input. How this problem is overcome? 10
- (b) With the help of suitable block diagram, explain working of Successive Approximate Register (SAR) ADC. 10
- 5 (a) With the help of circuit diagram and appropriate waveforms, explain common mode response of differential amplifier. 10
- (b) Consider 4-bit DAC with following measured output voltage with $V_{REF}=5V$. Find DNL and INL. Does this DAC provide 4-bit resolution? 10
- {0.00:0.3195:0.625:1.0375:1.325:1.5625:1.755:2.1875:2.5:2.8125:3.125:3.5875:3.75:4.0625:4.495:4.6875}
- 6 Write short notes on any four 20
- (a) Comparator Design
 - (b) Cyclic DAC
 - (c) Beta Multiplier
 - (d) Mixed Signal Layout Issues
 - (e) Representation of noise in circuits